REMARKS

In an Office Action mailed June 29, 2005, the specification was objected to, claims 1-4, 7-9, 11-13, and 16-20 were rejected under 35 U.S.C. § 103(a) in view of U.S Pat. No. 4,906,871 ("Iida"), claims 5, 6, 14, and 15 were rejected under 35 U.S.C. § 103(a) in view of Iida, claim 10 was rejected under 35 U.S.C. § 103(a) over Iida in view of Weste, Principles of CMOS VLSI Design: A Systems Perspective ("Weste"). These rejections are addressed in corresponding numbered paragraphs below.

1. Objection to the Specification

At page 2, paragraph 1 of the Office Action, the specification was objected to as failing to provide proper antecedent basis for claims 5 and 14 "first and second transistors are characterized as having an oxide stress voltage less than said first voltage" and for claims 6 and 15 "first and second transistors are characterized as having a gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process."

An objective standard for determining compliance with the written description requirement is, "does the description clearly allow persons of ordinary skill in the art to recognize that he or she invented what is claimed." In re Gosteli, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). The subject matter of the claim need not be described literally (i.e., using the same terms or in haec verba) in order for the disclosure to satisfy the description requirement. See M.P.E.P. § 2163.02.

With regard to the oxide stress voltage, the term oxide stress voltage is described in the application such that a person of ordinary skill in the art would recognize that the inventor was in possession of the embodiment recited in the claims. The Application states:

> For example in modern complementary metal oxide semiconductor (CMOS) integrated circuit fabrication processes, it is common to have multiple gate oxide thicknesses to accommodate both high-voltage and low-voltage transistors. The thicker gate oxide of the high voltage transistors make them able to withstand higher gate voltages without

> causing harmful stress to their gate oxide. Thus they may be used in higher voltage circuits.

Application, p. 1, paragraph 0003. Additionally, the Application states:

> By choosing C_{42} to be a little larger than C_{gs}, the voltage swing at node 43 can be reduced to about 1.2 V, which is small enough to avoid stressing low voltage transistors 44 and 45.

Application, p. 5, paragraph 0017.

The Application provides that buffer 40 translates an AC input signal having relatively high peak-to-peak voltage swing provided by signal source 30 to node 41 into a second signal having a smaller peak-to-peak voltage swing at node 47 (see Application, p. 5, paragraph 0016). Consequently, the input to the buffer 40 has a reduced voltage swing that is small enough to avoid stressing low voltage transistors 44 and 45. Thus, the term oxide stress voltage is outlined in the disclosure in sufficient detail that a worker skilled in the art would appreciate that the inventor was in possession of the claimed subject matter. Therefore, the objection to the application is improper and should be withdrawn.

With regard to claims 6 and 15, the specification addresses the issue of oxide thicknesses in relation to higher gate voltages (See Application, page 1, paragraph 0003). The Application states:

> For example in modern complementary metal oxide semiconductor (CMOS) integrated circuit fabrication processes, it is common to have multiple gate oxide thicknesses to accommodate both high-voltage and low-voltage transistors. The thicker gate oxide of the high voltage transistors make them able to withstand higher gate voltages without causing harmful stress to their gate oxide. Thus they may be used in higher voltage circuits. For example, a digital input buffer may use high-voltage transistors to receive an external signal that varies between 0 and 3.0 volts.

Application, p. 1, paragraph 0003. Additionally, the Application specifies that faster low voltage transistors 44 and 45 can be used within buffer 40 (See Application, pp. 4-5, paragraph 0016).

Thus, transistors with thick gate oxide layers can be used for high voltage applications, while less thick oxide layers can be used in faster, low-voltage transistors. However, with this

response, Applicants have amended the application at page 5, paragraph 0016 to include the following sentence:

> In one embodiment, transistors 44 and 45 have a gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process.

No new matter is added, since the text of the sentence was included in the claims as originally filed, and the paragraph to which the sentence is added already included a reference that the buffer 40 can use faster low-voltage (e.g. thinner gate oxide) transistors. Thus, the objection to the specification is overcome and should be withdrawn.

2. *Iida Fails to Disclose or Suggest All of the Elements of Claims 1-4, 7-9, 11-13, and 16-20.*

At page 2 of the Office Action, claims 1-4, 7-9, 11-13, and 16-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Iida. Applicants traverse.

Claims 1 and 8 recite a capacitor having a first terminal for receiving an input signal, wherein the input signal has a peak-to-peak voltage swing equal to a first voltage. Additionally, claim 1 recites a first transistor comprising a low-voltage transistor having a first current electrode coupled to a first supply voltage terminal for receiving a first power supply voltage, a second transistor comprising a low voltage transistor having a first current electrode coupled to a second current electrode of the first transistor, and a second current electrode coupled to a second power supply voltage terminal for receiving a second power supply voltage, wherein a voltage difference between the first and second power supply voltages is equal to a second voltage that is lower than the first voltage and wherein a capacitance of the capacitor is chosen such that a peak-to-peak voltage swing at control electrodes of the first and second transistors is less than or equal to the second voltage.

As discussed above, this reduction of input voltage swing to the control electrodes of the transistors is advantageous in that it allows for minimal oxide thicknesses, and therefore faster, low-voltage transistors. See Application, p. 1, paragraph 0003, and page 4-5, paragraph 0016. Moreover, the faster low-voltage transistors reduce the loading seen by the signal source 30 and hence power consumption.

The Office Action points to circuit 14 in FIG. 3 of Iida as being a level shifter (See Office Action, p. 3, paragraph 3). Specifically, the Office Action states:

> The Iida reference does not disclose the amplitude of level shifter 14 is lower than the amplitude of the input signal of the circuit 14 (i.e., the second voltage is lower than the first voltage). However, it is known in the art that a level shifter is used to interface between two different circuits/systems having different amplitudes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify each of the circuit 14 in Figures 3 and 5-7 of the Iida reference by specifically using the input signal of the circuit 14 having an amplitude greater than the amplitude of the output signal of the circuit 14 for the purpose of interfacing between a system having a higher amplitude signal and another system having a lower amplitude signal. Note that the use of a level shifter circuit to transform a higher amplitude signal to a lower amplitude signal and vice versa is depending on the need of the circuit designer for a specific application. This is deemed to be a routine design expedients (sic) for those having ordinary skill in the art of the CMOS buffer/shifter design. Thus, this modification meets all the limitations of these claims including the second voltage (amplitude of the output voltage) is less than the first voltage (amplitude of the input voltage), and a capacitance of capacitor (19) is chosen such that the peak-to-peak voltage swing at the control electrodes of the first and second transistors (amplitude of signal voltage V1 in Figure 3, and amplitude of the node at the gates Q5-Q6 in Figures 5-7) is less than or equal to the second voltage (because of the drop across feedback resistor R5 in Figure 3, Q7 and/or Q8 in Figures 5-7).

See Office Action, pp. 3-4, paragraph 3.

Applicants respectfully disagree. First, Iida does specify that the input voltage V1 is approximately 0.4 volts, while the output voltage V2 is approximately 4.4 volts (See Iida, Col. 2, lines 60-64, and Col. 3, lines 31-47). Thus, Iida does specifically disclose that the amplitude of the level shifter is greater than the amplitude of the input to the circuit, by a factor of 10.

Second, Applicants submit that the output V2 of the inverter circuit 14 of Iida is not equivalent to the second voltage as recited in claims 1 and 8. Specifically, claims 1 and 8 recite that a voltage difference between said first power supply voltages and said second power supply voltage is equal to a second voltage. Within claims 1 and 8, this second voltage is not indicated to be an output voltage of the buffer, but rather the voltage difference between the supply voltages applied to the first and second transistors. Moreover, claims 1 and 8 recite a peak-to-peak voltage swing at said control electrodes of said first and second transistors is less than or

equal to said second voltage. Thus, the second voltage does not necessarily appear at the circuit output, as suggested by the Office Action. Moreover, the Office Action asserts that

> the peak-to-peak voltage swing at the control electrodes of the first and second transistors (amplitude of signal V1 in Figure 3 and amplitude of the node at the gates of Q5-Q6 in Figures 5-7) is less than or equal to the second voltage (because of the drop across feedback resistor R5 in Figure 3, Q7 and/or Q8 in Figures 5-7), see Col. 3, lines 30-46 for more detail.

See Office Action, p. 3.

Applicants respectfully disagree with the asserted interpretation of Iida. At the cited passage, Iida states:

> The operation of the circuit in FIG. 3 will be described. The output of the signal of ECL prescaler 13, which derived from the collector of transistor T1, has an amplitude of approximately 0.4 V. When this signal is applied to the first electrode of capacitor 19, it is applied to the second electrode of the capacitor through its capacitive coupling path, and in turn to the input node of CMOS inverter 20. Bias resistor R5 is connected between the input node and the output node of CMOS inverter 20, and provides a predetermined bias voltage to the input node.

Iida, Col. 3, lines 30-40.

Thus, Iida teaches that the bias resistor R5 is connected between the input and the output voltage. The second voltage, recited in claims 1 and 8, is a difference between supply voltages, not the output voltage of the buffer. Thus, the presence of the bias resistor R5 between the input and the output of circuit 14 has nothing to do with whether the difference between supply voltages is greater than the peak-to-peak input. Thus, the cited passage is irrelevant with regard to a peak-to-peak voltage swing at said control electrodes of said first and second transistors being less than or equal to said second voltage, as provided in claims 1 and 8. Iida fails to disclose or suggest a second voltage or a peak-to-peak voltage swing at the control electrodes of the first and second transistors that is less than or equal to the second voltage.

Furthermore, Applicants submit that the capacitance value chosen for the capacitor is more than a design expedient. The capacitor is chosen to reduce the inputs to the control electrodes of the transistors to be within a range specified by a difference between the first and second supply voltages (the second voltage), as recited in claims 1 and 8. This reduction allows for use of faster low-voltage transistors while reducing the loading seen at the first terminal by a

signal source. See Application, p. 5, paragraph 0016. Iida fails to disclose or suggest either the sizing of capacitor 19 to achieve this reduction in peak-to-peak voltage, or the use of low-voltage transistors.

Applicants submit that the issue of oxide stress voltage, which is of concern in low-voltage transistors, is not addressed or at issue in Iida. This may be, in part, because circuit 14 in Iida is an inverting circuit coupled to a differential amplifier, where the gate bias voltage range of the MOS transistors is determined based on the resistance of resistors R3 and R4 of the ECL receiver 13 and based on the current source I_B (See Iida, Col. 1, lines 35-38). Thus, circuit 14 is exposed to a signal from a differential amplifier, which has a low peak-to-peak voltage, and therefore there is no need to be concerned with gate oxide stress. Additionally, Iida fails to disclose or suggest that the transistors Q5 and Q6 are low-voltage transistors, as provided in claim 1. As discussed above, thick oxide transistors can handle higher voltages. Thus, problems solved by teachings of the Application were not contemplated by Iida. Therefore, the modification of circuit 14 to resolve such problems would not be an obvious design consideration.

The circuit 14 is designed to overcome parameter variance and power voltage variation in the ECL (See Iida, Col. 1, lines 31-44). Capacitor 19 "blocks transfer of the DC like voltage variation due to the parameter variance and power voltage variation." (See Col. 1, line 66-Col. 2, line 1). Thus, the capacitance of capacitor 19 is used to block DC voltage variations, and not to reduce peak-to-peak voltage swing at the control electrodes. Iida fails to disclose or suggest a capacitance of said capacitor chosen such that a peak-to-peak voltage swing at said control electrodes of said first and second transistors is less than or equal to said second voltage, as recited in claims 1 and 8.

In light of the above-remarks, it should be apparent that Iida fails to disclose or suggest all of the elements of independent claims 1 and 8. Therefore, the rejection of claims 1 and 8 over Iida is improper and should be withdrawn.

Claims 2-4 and 7 depend from independent claim 1, and claims 9, 11-13, and 16 depend from claim 8. Therefore, Iida fails to disclose or suggest all of the elements of claims 2-4, 7, 9, 11-13, and 16, at least by virtue of their dependency from allowable independent claims 1 and 8. Therefore, the rejection of claims 2-4, 7, 9, 11-13, and 16 should be withdrawn.

Claim 17 recites a method of buffering an input signal having a peak-to-peak voltage equal to a first voltage, *capacitively dividing the first voltage using a capacitive divider formed by a capacitor having a first terminal for receiving the input signal and a second terminal in series with a parasitic capacitance formed by control electrodes of first and second transistors to provide a second signal at said second terminal of said capacitor having a peak-to-peak voltage equal to a second voltage,* and *buffering said second signal using a buffer including said first and second transistors driven by a power supply voltage that is less than said first voltage and greater than or equal to said second voltage.*

As previously discussed, Iida fails to disclose or suggest a second signal at the second terminal of the capacitor having a peak-to-peak voltage that is less than the first voltage and greater than or equal to the second voltage. Thus, Iida fails to disclose or suggest all of the elements of independent claim 17.

Claims 18-20 depend from allowable independent claim 17. Therefore, Iida fails to disclose or suggest all of the elements of claims 18-20, at least by virtue of their dependency from independent claim 17. Therefore, the rejection of claims 17-20 over Iida is improper and should be withdrawn.

3. Iida and Guedon Fail to Disclose or Suggest All of the Elements of Claims 5, 6, 14, and 15.

The Office Action acknowledges that Iida fails to disclose or suggest that "the first and second transistors having gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process." (*Office Action*, p. 5). The Office Action asserts that Guedon teaches use of only thin gate-oxide transistors provides the advantage of making the device more compact (*See Office Action*, p. 5).

However, Applicant notes that in light of the discussion above, Iida fails to disclose all of the elements of the independent claims. Like Iida, Guedon fails to disclose a capacitor having a first terminal for receiving an input signal, wherein the input signal has a peak-to-peak voltage swing equal to a first voltage, a first transistor comprising a low-voltage transistor having a first current electrode coupled to a first supply voltage terminal for receiving a first power supply voltage, a second transistor comprising a low voltage transistor having a first current electrode coupled to a second current electrode of the first transistor, and a second current electrode

coupled to a second power supply voltage terminal for receiving a second power supply voltage, *wherein a voltage difference between the first and second power supply voltages is equal to a second voltage that is lower than the first voltage* and *wherein a capacitance of the capacitor is chosen such that a peak-to-peak voltage swing at control electrodes of the first and second transistors is less than or equal to the second voltage.* Therefore, the combination of Iida and Guedon fails to disclose or suggest all of the elements of claim 1 and 8, and therefore fails to disclose or suggest all of the elements of claims 5, 6, 14, and 15, at least by virtue of their dependency from claims 1 and 8. The rejection of claims 5, 6, 14, and 15 over the combination of Iida and Guedon is improper and should be withdrawn.

4. Iida and Weste Fail to Disclose or Suggest All of the Elements of Claim 10.

The Office Action asserts that the Iida as applied to claims 8 and 9 above meets all of the limitations of claim 10 "except that the load is a capacitor connected between the second end of the interconnect line and ground." (*See Office Action*, pp. 5-6, paragraph 5).

Applicants disagree. Iida fails to disclose all of the elements of independent claim 8 from which claim 10 depends. Like Iida, Weste fails to disclose a capacitor having a first terminal for receiving an input signal, wherein the input signal has a peak-to-peak voltage swing equal to a first voltage, a first transistor comprising a low-voltage transistor having a first current electrode coupled to a first supply voltage terminal for receiving a first power supply voltage, a second transistor comprising a low voltage transistor having a first current electrode coupled to a second current electrode of the first transistor, and a second current electrode coupled to a second power supply voltage terminal for receiving a second power supply voltage, *wherein a voltage difference between the first and second power supply voltages is equal to a second voltage that is lower than the first voltage* and *wherein a capacitance of the capacitor is chosen such that a peak-to-peak voltage swing at control electrodes of the first and second transistors is less than or equal to the second voltage.* Therefore, the combination of Iida and Weste fail to disclose or suggest all of the elements of claim 10. The rejection of claim 10 over the combination of Iida and Weste is improper and should be withdrawn.

5. The Cited Art Fails to Disclose or Suggest All of the Elements of New Claims 21-23.

New claims 21 and 22 are added. Claims 21 and 22 depend from allowable independent claims 1 and 8, respectively, and recite that the capacitance of the capacitor is greater than a combined parasitic capacitance of the first transistor and the second transistor. The cited references, alone or in combination, fail to disclose or suggest all of the elements of claims 21 and 22. Therefore, claims 21 and 22 are allowable over the cited art. Consideration and notice to that effect is respectfully requested.

New claim 23 is added to depend from allowable independent claim 17. Claim 23 recites the circuit of claim 17 wherein the capacitor comprises a capacitance that is greater than the parasitic capacitance. None of the cited references, alone or in combination, disclose or suggest all of the elements of claim 23. Therefore claim 23 is allowable, and consideration and notice to that effect is respectfully requested.

6. The Specification and Claims were Amended to Correct Informalities.

Applicants correct a reference number error in paragraph [0015] of the Specification. In addition, Applicants correct an informality in claim 10.

CUSTOMER NO.
34456

CONCLUSION

Applicants respectfully submit that the amendment of September 22, 2005 is now compliant. Accordingly, the Examiner is requested to withdraw all of the rejections in light of the above remarks and to issue a Notice of Allowance for all pending claims. If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney or agent.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

10/25/05
Date

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No. 10/809,195	Applicant(s)	
	Examiner Nguyen, Long	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on 9/22/05 is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- [X] 1. Amendments to the specification:
  - [X] A. Amended paragraph(s) do not include markings.
  - [ ] B. New paragraph(s) should not be underlined.
  - [ ] C. Other _____.
- [ ] 2. Abstract:
  - [ ] A. Not presented on a separate sheet. 37 CFR 1.72.
  - [ ] B. Other _____.
- [ ] 3. Amendments to the drawings:
  - [ ] A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
  - [ ] B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
  - [X] C. Other _____.
- [X] 4. Amendments to the claims:
  - [ ] A. A complete listing of all of the claims is not present.
  - [ ] B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
  - [X] C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
  - [ ] D. The claims of this amendment paper have not been presented in ascending numerical order.
  - [X] E. Other: See Attachment

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714 and the USPTO website at http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/officeflyer.pdf .

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period** if the non-compliant amendment is an after-final amendment or an amendment filed after allowance. If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted within the time period set forth in the final Office action.
2. Applicant is given **one month**, or thirty (30) days, whichever is longer, from the mail date of this notice to supply the **corrected section** of the non-compliant amendment in compliance with 37 CFR 1.121, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a *Quayle* action.

Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

Failure to timely respond to this notice will result in:
Abandonment of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or
Non-entry of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

Annette Smith — Legal Instruments Examiner (LIE)

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